AF/GAU 2822

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes

Title: SILICON-GERMANIUM DEVICES FOR CMOS FORMED BY ION IMPLANTATION AND SOLID PHASE EPITAXIAL REGROWTH

Docket No.: 303.229US2
Filed: August 11, 1998
Examiner: Mark V. Prenty

Serial No.: 09/132,157
Due Date: January 30, 2001
Group Art Unit: 2822

Box AF
Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X An Amendment and Response After Final (7 Pages).

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: _____
Atty: David C. Peterson
Reg. No. P-47,857

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Box AF, Commissioner for Patents, Washington, D.C. 20231, on this 22 day of December, 2000.

Tina Pugh
Name

_____
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Customer Number 21186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)
(GENERAL)

EXPEDITED PROCEDURE - EXAMINING GROUP 2822

S/N 09/132,157 **PATENT**

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Serial No.:	09/132,157	Group Art Unit: 2822	
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#22 L Saylor 1/3/01

AMENDMENT & RESPONSE UNDER 37 C.F.R. § 1.116

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In response to the Final Office Action mailed October 30, 2000, please amend the application as follows.

IN THE CLAIMS

Please cancel claims 30-31 without prejudice or disclaimer. Please amend claims 11, 24, 25, 28, 32, 38-41, and 43 as follows. Claims 11, 13-14, 24-28, 32, 38-43 are now pending in the application.

11. (Five times amended) A p-channel metal-oxide-semiconductor transistor, comprising:

a silicon substrate;

a silicon dioxide (SiO_2) gate oxide, coupled to the substrate;

a gate, coupled to the SiO_2 gate oxide;

source/drain regions formed in the substrate on opposite sides of the gate; and

a $Si_{1-x}Ge_x$ channel region, having a germanium molar fraction x, located underneath [and formed in the substrate, underneath and adjoining] the SiO_2 gate oxide and between the source/drain regions[;], wherein x is less than or equal to 0.6, and wherein the $Si_{1-x}Ge_x$ channel region forms a $Si_{1-x}Ge_x/SiO_2$ gate oxide interface.

[wherein the $Si_{1-x}Ge_x$ channel region has a channel length less than 7μm.]

24. (Five times amended) A p-channel metal-oxide-semiconductor transistor formed on a silicon substrate, comprising: